Remarks

In the Office Action dated December 29, 2005 which was made **FINAL** ("Final Rejection"), Claims 1, 2, 4-6, 12-16, 19-24, 29-32 and 34-36 were rejected and Claims 3, 7-11, 17, 18, 25-28, 33 and 37 were objected to, as follows.

1. Claim 14 was objected to for failing to provide proper antecedent basis for the phrase "other linked request" in line 6. The word "any" has been inserted before this phrase in line 6 to provide the appropriate antecedent basis, as suggested by the Examiner. In view of this amendment to the Claim, this objection should be withdrawn. Similarly, the objection to Claims 15-19, which depend from Claim 14, should likewise be withdrawn.

2. Claims 1, 2, 4-6, 12-16, 19-24, 29-32, and 34-36 were rejected under 35 USC §102(e) as being anticipated by U.S. Patent No. 6,434,641 to Haupt et al. ("Haupt"). This rejection is respectfully traversed.

As set forth in a previous response filed on October 12, 2005 ("Prior Response"), the system of Haupt differs from Applicants' claimed invention in at least one key respect. In Haupt, the memory creates a linked list of requested after the requests have been received by the memory from the processors. For example, in Haupt Figure 1, Memory Storage Units (MSUs) 110 provide the memory for the system. The MSUs receive requests from processors within PODs 120 via the MSU interfaces (MIs) 130. If any two requests are received by the MSUs that request the same data, the MSUs create a linked list of these requests.

In contrast to Haupt, Applicants' invention includes a main memory system called the Storage Coherency Director 100 that receives requests from processing nodes 120. The processing nodes 120 include one or more instruction processors. According to Applicants' invention, the processing nodes

create a linked list of requests before any requests are transferred to the memory. This conserves interface bandwidth, eliminates the need to process the duplicate requests within the memory, and prevents "data thrashing" wherein data is transferred multiple times between the memory and a processing node.

It may be noted that Applicants' invention is not merely an obvious modification of the system shown in Haupt. Applicants' processing nodes must handle linked requests in a manner that depends on the type of access rights granted to the processing node for a particular data item, as well as on the type of rights that are requested by a next linked request. The circuitry required to handle this task is non-trivial, as described throughout Applicants' Specification. In contrast, the processing of a linked request within the memory complex of Haupt system is relatively straight-forward, consisting primarily of clearing a designator for a given linked request so that the request then becomes eligible for presentation to by the memory circuitry to the RAMs.

Applicants' invention must further address significant coherency issues not implicated by the Haupt system. For example, Applicants' system must ensure that while linked requests are being processed, data stored within the shared cache of a POD is maintained in a coherent state. This is non-trivial, as is described, in part, on pages 17 through 22 of Applicants' Specification.

Next, the specific language of the Claims is discussed. Claim 29 is discussed first for ease of discussion. This Claim appears as follows:

A data processing system comprising:

a memory;

a processing node coupled to the memory and having one or more requesters to generate requests for data to the memory, wherein the processing node includes a requesting tracking circuit to record, in time-order, requests issued for the same data, and to allow only one of the requests for the same data from being issued to the memory at a given time. (Claim 29, emphasis added.)

This Claim recites a processing node that includes requesters to generate requests for data. The processing node includes a requesting tracking circuit to allow only one of the requests for the same data to be issued to the memory at a given time.

The Examiner cites element 250 of Haupt Figure 2, also referred to as the Memory Controller 250, as teaching the processing node. This Haupt "processing node" (i.e., the MCA) is contained within the main memory (i.e., the Haupt Memory Storage Unit, or MSU, 110.) This "processing node" does not contain any requesters that generate requests for data. Instead, the MCA of the MSU merely buffers part of the request. The request itself is generated by a Haupt processing module 120 (POD). This is described as follows:

> "...**MCA 250 buffers the address and control signals** associated with a memory request until the request may be routed to the addressed one of the MCLs 235. The [request] **address and controls signals are received from a respective one of the PODs** 120 on an associated one of the Address/command Lines 220, ..."(Haupt column 10 lines 25-30, emphasis added.)

Thus, Haupt does not teach any "processing node" element that includes both requesters to generate requests and a request tracking circuit of the type claimed by Claim 29.

For at least the foregoing reason, Haupt does not teach each and every element of Applicants' claimed invention, and Claim 29 is allowable over this rejection, which is improper, and should be withdrawn.

Claims 30-33 depend from Claim 29 are likewise allowable over the current rejection for at least the reasons discussed above in regards to Claim 29, and this rejection should be withdrawn in regards to this Claim.

Turning next to the remaining independent Claims, these Claims include aspects similar to those discussed above in regards to Claim 29. For example, Claim 1 describes how requests for the same data are recorded by a linked list (step b), and then one of the requests recorded by the linked list is issued from the processing node to the memory (step c). Moreover, Claim 1 step b.) recites that the linked list is included within the processing node. Neither of these aspects is taught by Haupt. For instance, in Haupt, the linked list is formed in the Memory Storage Unit (MSU). This MSU most certainly does not teach Applicants' processing node of Claim 1 for at least the reason that this MSU does not have multiple processors. Additionally, Haupt does not teach forming the linked list first, and only then issuing one of the requests contained in the list from the processing node to the memory. For at least these reasons, Claim 1 is allowable over this rejection.

Claims 2 – 11 depend from Claim 1 and are allowable over the current rejection for at least the reasons set forth in regards to Claim 1.

Next, independent method Claim 12 is considered. This Claim recites linking a request for data to another pending request before the other request

has been provided from the requester to the memory. This is not taught by Haupt, since Haupt never links any requests until after those requests are provided to the memory. Claim 12 is therefore allowable over the current rejection.

Claims 13 – 19 depend from Claim 12 and are allowable over the current rejection for at least the reasons set forth in regards to Claims 1 and 12.

Independent Claim 20 describes a system wherein a requesting tracking circuit associates requests for the same data with one another so that a single request for any given data from the requesters will be pending within the memory at a given time. As discussed above, in Haupt, all requests for the same data are provided by the requesters to the memory, and only then is the linked list formed to manage these requests. Thus, Haupt does not teach this aspect of Claim 20.

In addition to the foregoing, Claim 20 describes that the multiple requests and the request tracking circuit are included in the processing node. This is not taught by Haupt, as previously discussed in regards to Claim 29. For this additional reason, amended Claim 20 is allowable over this rejection.

Claims 21-28 depend from Claim 20 and are allowable over this rejection for at least the reasons discussed above in regards to other independent Claims 1, 13, and 29.

Finally, independent Claim 34 describes request tracking means for forming an association between any requests for the same data, and for then allowing only one of the associated requests to be provided from the processing means to the memory. In the Final Rejection, the Examiner cites POD 120 of Haupt as teaching the processing means of Claim 34. In Haupt, all requests for the same data are issued from the Haupt POD 120 to the memory 110. Only after memory 110 receives all requests does the memory create the linked list.

Thus, Haupt does not teach Applicants' Claim 34 wherein only one request for the same data is allowed to be provided from the processing means to the memory. For at least this reason, Claim 34 is allowable over this rejection.

Claims 35-37 depend from Claim 34 and are allowable over this rejection for at least the reasons discussed above in regards to Claim 34.

Conclusion

In the Office Action dated December 29, 2005 which was made **FINAL**, Claims 1, 2, 4-6, 12-16, 19-24, 29-32 and 34-36 were rejected and Claims 3, 7-11, 17, 18, 25-28, 33 and 37 were objected to. In view of the amendments to the Claims and the comments set forth above, it is submitted that all Claims are in condition for allowance, and a Notice of Allowance is respectfully requested. If the Examiner has any questions or concerns regarding the foregoing, a call to the undersigned is encouraged and welcomed.

Respectfully submitted,

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